REMARKS

Claims 1-28 are pending in the present application, were examined and stand rejected. In response, Claims 1, 8, 15 and 22 are amended, no claims are cancelled and no claims are added. Applicant respectfully requests reconsideration of pending Claims 1-28 in view of at least the following remarks. Reconsideration and withdrawal of the rejections of record are requested in view of such amendments and the following discussion.

I. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 1-28 under 35 U.S.C. §103(a) as being unpatentable over "Enhanced Code Compression for Embedded RISC Processors," by Cooper et al. ("Cooper") in view of U.S. Patent No. 6,918,111 issued to Damron et al. ("Damron"). Applicant respectfully traverses this rejection.

Regarding Claims 1 and 15, Claims 1 and 15 are amended to recite the following claim feature, which is neither taught nor suggested by the combination of Cooper in view of Damron:

> identifying a plurality of fork subgraph structures within a graph structure constructed for a plurality of executable instructions;
> identifying, prior to register allocation, a plurality of unifiable variables within each fork subgraph structure of said plurality of fork subgraph structures, which are not simultaneously used in said plurality of executable instructions;
> constructing a dependence graph of said plurality of executable instructions;
> using said dependence graph to identify at least one unifiable instruction of said plurality of executable instructions, within said plurality of fork subgraph structures; and
> transferring said at least one unifiable instruction of said plurality of executable instructions from a tine of a corresponding fork subgraph structure of said plurality of fork subgraph structures to a handle of said corresponding fork subgraph structure. (Emphasis added.)

In contrast to the above-recited features of amended Claims 1 and 15, which identify the plurality of unifiable variables prior to register allocation, Cooper teaches:

> In contrast to other methods, our framework preserves the ability to run program executables directly, without an intervening decompression stage. Our compression framework is integrated into an industrial-strength optimizing compiler, which allows us to explore the interaction between code compression and classical code optimization techniques, and requires that we contend with the difficulties of compressing previously optimized code. (pg. 139, left col., lines 13-21.) (Emphasis added.)

Based on the cited passage above, Applicant respectfully submits that the teachings of Cooper are directed to the difficulties of a compressing previously-optimized code. Applicant's argument is further substantiated by the following passage of Cooper:

> This paper explores one technique for reducing code size—code compression during the late stages of compilation. (pg. 139, right col., lines 16-18.) (Emphasis added.)

As further described by Cooper regarding the compression framework:

> Since our compression framework performs its work after the input code has been register-allocated, all interference graphs will be completely colored, with a distinct physical register (color) assigned to each live range. (pg. 143, left col., lines 37-41.) (Emphasis added.)

Hence, based on the above-cited passages, Applicant respectfully submits that Cooper fails to teach or suggest identifying, prior to register allocation, a plurality of unifiable variables within each subfork subgraph structure of said plurality of fork subgraph structures, which are not simultaneously used in said plurality of executable instructions, as recited by amended Claims 1 and 15.

As correctly recognized by the Examiner:

> Cooper does not explicitly disclose constructing a dependence graph of said plurality of executable instructions and using said dependence graph to optimize code execution. (pg. 4, ¶1 of the Office Action mailed November 3, 2005.)

As a result, the Examiner cites Damron at col. 4, lines 60-65. (*See*, pg. 4, ¶2 of the Office Action mailed November 3, 2005.)

As indicated by the passage referred to by the Examiner of Damron:

> As is well known in the art dependency graphs, and in particular directed acyclic graphs (DAGs) are commonly used to map or graph dependencies between instructions. Dependency graphs have been used in the past to help optimize instruction scheduling for processor pipelines, or processors with multiple execution units. (col. 4, lines 60-65.) (*See*, pg. 4, ¶2 of the Office Action mailed November 3, 2005.) (Emphasis added.)

Applicant respectfully submits that the teachings of Cooper are directed to a compression framework, which performs its work after input code has been register allocated (*see*, supra) and it is designed to contend with the difficulties of compressing previously-optimized code and exploring techniques for code compressing during late stages of compilation. (*See* Cooper, pg. 139, left col., lines 13-21 and pg. 139, right col., lines 16-

18.) Hence, since Cooper is neither directed to optimizing instruction scheduling for processor pipelines or processors with multiple execution units, Applicant respectfully submits that one skilled in the art would not incorporate the teachings of Damron into the system of Cooper to construct a data dependence graph of said plurality of executable instructions and using said graph to optimize code execution, as indicated by the Examiner. Such a modification would not be made by one skilled in the art, since Cooper is directed to reducing the size of optimized code by performing code compression during the late stages of compilation. (*See*, pg. 139, right col., lines 16-18.)

As mandated by case law, "to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Here, the disclosure in Cooper is directed to a compression framework, which is designed to contend with difficulties of compressing previously-optimized code and explores one technique for reducing code size by performing code compression during the late stages of compilation. (*See*, Cooper, pg. 139, left col., lines 16-21 and right col., lines 16-18.) Accordingly, Applicant respectfully submits that Cooper, based on the explicit recitation provided above, fails to teach or suggest identifying, prior to register allocation, a plurality of unifiable variables within each fork subgraph structure of said plurality of fork substructures, which are not simultaneously used on said plurality of executable instructions, as recited by amended Claims 1 and 15.

Regarding the Examiner's citing of Damron, Applicant respectfully submits that the Examiner's citing of Damron fails to rectify the deficiencies of Cooper to each teach or suggest the identification, prior to register allocation, of unifiable variables within each subfork prior to register allocation, as recited by amended Claims 1 and 15. Consequently, Applicant respectfully submits that the combination of Cooper in view of Damron fails to teach or suggest all of the above-recited features of amended Claims 1 and 15, as required to establish a *prima facie* case of obviousness. Id.

Furthermore, Applicant respectfully submits that one skilled in the art would not incorporate the teachings of Damron to the system of Cooper to construct a data dependence graph dependency graphs are generally used for optimizing instruction scheduling for

processor pipelines or processors with multiple execution units. Conversely, Cooper is directed to a compression framework, which contends with difficulties of compressing previously optimized code and therefore explores one technique for reducing code size by using code compression during the late stages of compilation. (*See*, pg. 139, left col., lines 15-21 and right col., lines 16-18.) As further recited by Cooper, the compression framework performs its work after the input code has been register allocated. (pg. 143, left col., lines 37-41.)

Accordingly, since the disclosure in Cooper is directed to compression of previously-optimized code, or at least compression during the later stages of compilation when optimization has already been performed, one skilled in the art would not modify Cooper, as taught by Damron, to provide a dependency graph, as required to render amended Claims 1 and 15 obvious. Therefore, Applicant respectfully submits that the Examiner has engaged in a hindsight-based analysis to modify the disclosure of Cooper with the construction of a data dependence graph, as taught by Damron.

Consequently, Applicant respectfully submits that for at least the reasons provided above, Applicant respectfully submits that the combination of Damron in view of Cooper would neither suggest that the claimed subject matter to one of ordinary skill in the art is required to establish a *prima facie* case of obviousness. In re Rijckaert, 9 F.3d 1531, 28 U.S.P.Q. 2d 1955 (Fed. Cir. 1993).

Therefore, for at least the reasons provided above, Applicant respectfully submits that amended Claims 1 and 15 are patentable over the combination of Damron in view of Cooper. Id. Hence, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 1 and 15.

Regarding Claims 2-14, Claims 2-14, based on their dependency from Claim 1, are also patentable over the combination of Cooper in view of Damron. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 2-14.

Regarding Claims 16-21, Claims 16-21, based on their dependency from Claim 15, are also patentable over the combination of Cooper in view of Damron. Consequently,

Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 16-21.

Regarding Claims 8 and 22, Claims 8 and 22 recite the following analogous claim feature:

> identifying, prior to register allocation, a plurality of unifiable variables within each fork subgraph structure of said plurality of fork subgraph structures. (Emphasis added.)

Applicant respectfully submits that the above-recited feature of amended Claims 8 and 22 is analogous to the above-recited feature of amended Claims 1 and 15.

Accordingly, Applicant's arguments provided above with regard to the §103(a) rejection of Claims 1 and 15 as obvious over Cooper in view of Damron, equally apply to the Examiner's §103(a) rejection of Claims 8 and 22 as obvious over the indicated prior art. Accordingly, for at least the reasons provided above, Applicant respectfully submits that Claims 8 and 22, as amended, are patentable over the combination of Cooper in view of Damron, since such combination fails to teach or suggest each of the above-recited features of amended Claims 8 and 22. In re Royka, supra. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 8 and 22.

Regarding Claims 9-14, Claims 9-14, based on their dependency from Claim 8, are also patentable over the combination of Cooper in view of Damron. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 9-14.

Regarding Claims 23-28, Claims 23-28, based on their dependency from Claim 22, are also patentable over the combination of Cooper in view of Damron. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 23-28.

CONCLUSION

In view of the foregoing, it is submitted that Claims 1-28, as amended, patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: February 02, 2006

By: _____
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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 02, 2006

Marilyn Bass February 02, 2006